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(71) Applicant: ITALTEL S.P.A [IT/IT]; Piazzale Zavattari, 12, I-20149 Milano (IT).

(72) Inventors: CARCANO, Giorgio; Via G. Parini, 106, I-20043 Arcore (IT). LAZZARI, Stefano; Viale Casiraghi, 491, I-20099 Sesto S. Giovanni (IT). MAGLIOCCO, Massimo; Via Iseo, 10, I-20052 Monza (IT).

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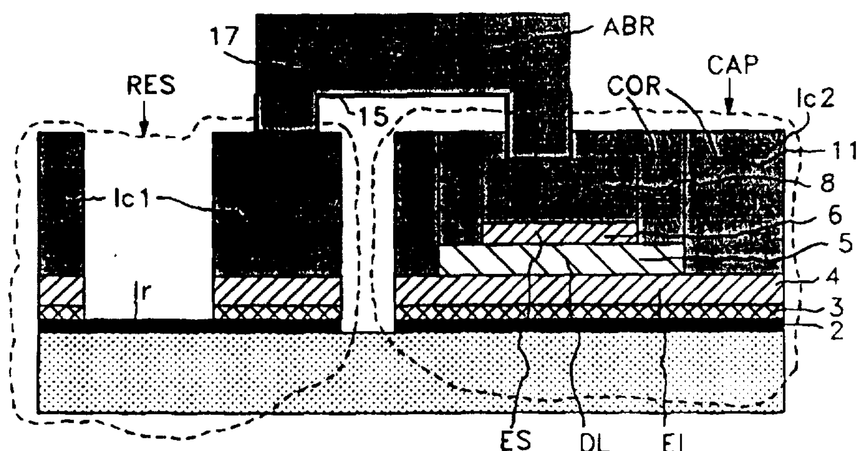

(57) Abstract

There is described a manufacturing process for thin-film circuits comprising the phases of: a) sputtering of superimposed layers of TaN, Ti, Pd^1, Ta_2O_5 and Pd^2 (2, 3, 4, 5, 6) in a single vacuum cycle, b) photoetching of the Pd^2 layer and creating upper electrodes (ES) of capacitors (CAP), c) photoetching of the Ta_2O_5 layer and creation of respective dielectrics (DL) more extensive than the upper electrodes, d) photomasking and growth of galvanic gold (11) along conductive paths (1c1, 1c2) and a resistive path (1r) and opposite lower electrodes (EI) forming crowns (COR) which enclose the dielectrics, e) engraving of Pd^1, Ti and TaN outside the galvanic gold (11) to create the capacitors (CAP) and the conductive lines (1c1, 1c2), f) engraving of Au, Pd^1 and Ti opposite the resistive paths (1r) to create the resistors (RES), and g) execution of metallic air bridges (ABR) to interconnect the upper electrodes of the capacitors with the rest of the circuit.

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"Manufacturing process for thin-film circuits comprising integrated capacitors"

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DESCRIPTION

The present invention relates to the field of industrial processes for creating
5 hybrid thin-film circuits on dielectric substrates for microwave applications and specifically to a manufacturing process for thin-film circuits comprising integrated capacitors.

As known, in the above mentioned technical field one of the problems posed by the requirement to achieve more complete circuit integration is creating in a single
10 production process all the passive elements together with the conductive paths of the interconnections. Initially the processes of depositing thin films on dielectric substrates were predominantly aimed at creating resistors and inductors and conductive lines and excluded the capacitors, for which it was necessary to use chip components connected to the circuit by means of surface mounting techniques.
15 Subsequently, the thrust for the search for a greater integration led to the development of processes of deposit of thin films extending to the capacitors.

The integration of small capacitors with characteristics readily repeatable in the production process results in undoubted advantages among which are reduction of production costs, achievement of a greater degree of circuit miniaturization, the
20 faculty of better optimizing the layout, extension in frequency of the operating band of the associated circuits and reduction of parasite parameters.

In the article by G.P. Ferraris and R. May entitled "TANTALUM THIN FILM CAPACITORS WITH VARIOUS TYPES OF COUNTERELECTRODES", published in "Electrocomponent Science and Technology", Vol. 6, pages 235-240, year 1980,
25 published by Gordon and Breach Science Publishers, Inc, Great Britain, are set forth the measurement results of the principal electrical parameters of thin-film capacitors whose dielectric consists of a layer of tantalum pentoxide (Ta_2O_5), created by subjecting to a known electrolytic process (anodizing) a layer of tantalum (Ta) used as the lower electrode in capacitors. The Ta_2O_5 possesses a relative dielectric constant
30 around 25, which is much greater than that of the more common materials used for the same purpose and thus allows creating capacitors with high surface density of capacitance.

The above mentioned capacitors were developed by the same authors in the laboratories of the applicant, using a process which integrated on a single substrate
35 the tantalum resistive paths, the capacitors and the gold conductive paths.

The article investigates the possibility of reducing the resistivity of the tantalum layer constituting the material of the lower electrode of the integrated

capacitors, introducing a dopant nitrogen flow during the vacuum cathode tantalum sputtering.

The investigation continues by examining in addition the electrical characteristics of capacitors which differ only in the type of metal used in the
5 sputtering phase of the material constituting the upper electrode.

As concerns the first point, the results of the investigation are set forth in the quotation in Table 1 and FIG 1 on page 236, from which it appears that the doping with nitrogen effectively reduces the resistivity of the tantalum layer making up the lower electrode, while causing at the same time a change of sign and an increase in
10 the positive value of the temperature coefficient (TCR) of the layer and simultaneous reduction of the capacitance density of the capacitor. On the contrary, the requirement for having a TCR as near zero as possible together with high capacitance densities prevents minimization of the resistivity of the tantalum in this type of capacitor, which is therefore always characterized by high values of equivalent series
15 resistance (ESR).

Recalling that for a generic capacitor the value of the dissipation factor tan δ gives an idea of how much the electrical behaviour deviates from the ideal case, and that $\tan \delta = \tan \delta' + \omega C R_o$, where R_o = ESR and the term tan δ' allows for an intrinsic loss of the independent dielectric by the frequency, it can be noted that only the
20 presence of an ESR introduces a power dissipation which increases with the increase in frequency, ESR and capacitance.

From the foregoing it is clear that the great shortcoming of thin film circuits which integrate capacitors with Ta_2O_5 dielectric created by anodizing a tantalum layer previously deposited by photoengraving of the resistive paths, is to show a small
25 value (<10 kHz) in the upper limit of the operating frequencies. A partial remedy for this shortcoming consists of improving the conductivity of the lower electrode by means of a layer of aluminum underlying the tantalum layer as described for example in the article by L.G. FEINSTEIN and R.J. PAGANO entitled "Ta Thin-Film Capacitors with an Al Underlay for High-Frequency Application", published in "IEEE
30 TRANSACTIONS ON COMPONENT HYBRIDS, AND MANUFACTURING TECHNOLOGY", vol. CHMT-4, No. 1, March 1981. In the best of cases, with these methods the upper limit of the operating frequencies does not exceed 10 MHz, which is still a too low value for microwave applications.

The shortcoming of capacitors with anodized tantalum dielectric was known
35 even before disclosure of the above mentioned articles, as appears in patent application US 4038167, P.L. Young, inventor, with priority 9 February 1976, in which is explained a method of manufacturing a thin-film capacitor on a dielectric substrate

comprising in sequence the steps of:

- application of a first non-tantalum conductive film on the above mentioned dielectric substrate to form a first electrode of the capacitor;
- positioning of said substrate and the associated conductive film in a vacuum environment in which is introduced a gaseous mixture of oxygen and nitrogen;
- sputtering from tantalum pentoxide (Ta_2O_5) targets and deposit of an associated film of the desired thickness over said conductive film;
- cooling of said dielectric substrate and conductive film during deposit of the tantalum pentoxide, and subsequently
- application of a second non-tantalum conductive film to form a counter-electrode of the capacitor.

In the text and claims it is also stated that the conductive films making up the electrodes are of aluminum. It is necessary to specify that the method is addressed to the manufacture by sputtering of a capacitor with Ta_2O_5 dielectric, understood exclusively as a single component, and indeed nothing is said about how to integrate the method explained in a broader process for the manufacture of thin-film circuits comprising the capacitors, resistors and conductive lines. It must also be underlined that in the capacitors created by the above mentioned method there can easily occur short circuits between the electrodes, aided by the excessive nearness of the edges thereof, as may be seen in FIG 4, which shows a half-section of the capacitor consisting of the dielectric substrate with the three superimposed layers forming the capacitor, all of the same longitudinal dimension.

With respect to the capacitors created by the method of P.L. Young in which the Ta_2O_5 dielectric was created directly from Ta_2O_5 targets, the Ta_2O_5 dielectrics of the capacitors, integrated in thin-film circuits manufactured in conformity with the most recent manufacturing processes, are preferably created by performing a reactive sputtering from tantalum only in the presence of argon gas and oxygen. The problem of short circuits between the electrodes was solved my merely reducing the dimensions of the upper electrode with respect to the dielectric.

An example which illustrates the reactive Ta_2O_5 sputtering to create the dielectric of an integrated capacitor having greater surface area than that of the upper electrode is supplied in the article by A. Chu et al. entitled "A Two-Stage Monolithic IF Amplifier Utilizing a Ta_2O_5 Capacitor", published in "IEEE TRANSACTIONS ON ELECTRONIC DEVICES", VOL. ED-30, No 1, January, 1983. In FIG 4 of the article is given a sequence of steps of a manufacturing process of a monolithic integrated circuit (MMIC) operating at microwaves and where there is given greater emphasis to the production of a capacitor integrated in thin film placed between two GaAsFETs. In

the first two steps of the process the GaAsFETs are almost completed, while the subsequent steps concern predominantly the production of the capacitor and related connections. In step 3 are deposited in sequence five layers, namely: Au, Ta, Ta_2O_5, Ta and Au in a single vacuum cycle and exclusively in the area occupied by the
5 capacitor. In step 4 are partially etched the layers of Au and Ta deposited last, to create the upper electrode of the capacitor. In step 5 is partially etched the Ta_2O_5 on one side of the structure, uncovering in this manner a strip of the underlying metallization belonging to the lower electrode of the capacitor. The purpose is to create a zone for the subsequent anchoring of metallic connection lines. In step 6 is
10 deposited photosensitive polyimide which, after masking, exposure and development, acts as support material in the production of a metallic air bridge, connecting the upper electrode of the capacitor to a GaAsFET. In step 7 is deposited by sputtering a metallization which covers the gate zone of the GaAsFETs, the residual polyimide, the uncovered metallic strip belonging to the lower electrode and a contiguous substrate
15 zone starting close to the capacitor dielectric. In step 8 the electrolytic gold is grown on the preceding metallization but limited to the air bridge and along the paths corresponding to transmission lines or to those for connection to the capacitor. In step 9 the polyimide is removed and the sputtering metallization of step 7 is etched outside the electrolytic gold grown in step 8.

20 On page 22 of the article at the bottom of the first column it is stated that, concerning the layers deposited in step 3, the two tantalum layers serve to bond the Ta_2O_5 layer of the dielectric to the gold substrates of the electrodes, because without them adhesion of the Ta_2O_5 to the gold would be poor. It is also stated that, to minimize losses, the thickness of the tantalum layers should be held to the minimum
25 required for good adhesion. The solution proposed is general in nature in thin-film technology and consists of using an interface layer between two others which, if placed in direct mutual contact, would show problems of compatibility concerning some physical characteristics such as e.g. adhesion, or solid diffusivity or other. In the case analyzed, the adhesion is presumably promoted by the formation of a Ta-Au
30 alloy on one side of the interface and a Ta oxide with physical characteristics close to the Ta_2O_5 on the other side, where there can be seen a certain similarity with the anodized tantalum capacitors, which did not show any adhesion problem but had ohmic losses.

In thin-film circuit manufacturing processes allowing integration of the
35 capacitors with the rest of the layout, it may be advantageous to use the steps of the process of A. Chu described above, but inheriting their shortcomings, among which there is that of having to deposit two additional tantalum layers with only interface

functions and consequently that of not being able to fully utilize the good electrical conductivity of the gold of the electrodes, and thereby optimize the utilization band of the circuits as mentioned above. It is also pointed out that in the article in question nothing is said of the long-term mechanical stability of the capacitor structure, which is
5 indeed quite complex.

Accordingly the purpose of the present invention is to overcome the above mentioned shortcomings and indicate a manufacturing process for thin-film circuits on dielectric substrates by means of which it would be possible to create capacitors having great capacitance density, great production simplicity, excellent mechanical
10 and structural stability, and a very low dissipation factor making them suitable for microwave operation.

To achieve these purposes the present invention has for its subject matter a manufacturing process for thin-film circuits on a dielectric substrate consisting of the following phases:
15 - sequential cathode sputtering in a single vacuum cycle of metals which are deposited on the substrate to form superimposed layers and that is, in order, resistive, conductive, dielectric and conductive;

- definition of the geometry of upper electrodes of the capacitors and their creation by removal of material from the same conductive layer;
20 - definition of the geometry of dielectrics of the capacitors in surface zones more extensive than those of the corresponding upper electrodes and their creation by removal of material from the same dielectric layer;

- definition of the geometry of lower electrodes of the capacitors in surface zones more extensive than that of the corresponding dielectrics and galvanic growth
25 of gold along conductive and resistive paths and close to the edge of the dielectrics in zones lying between the edges of the dielectrics and the corresponding lower electrodes;

- etching of the metallizations outside the gold deposited electrolytically, to create the capacitors and conductive lines connected to the lower electrodes;
30 - etching of the metallizations of the conductive lines in correspondence of the resistive paths, excepting the metal belonging to the first resistive layer to create the resistors; and

- execution of metallic air bridges to interconnect the upper electrodes of the capacitors to the rest of the circuit as better described in the claims.
35 The metals used in the base layers are, in order, Ta, Ti, Pd, Ta and Pd, of which the tantalum of the first layer is doped with nitrogen, or nitrogen and oxygen, to aid deposit of a resistive layer. The titanium acts as an adhesive between the doped

Ta and the first Pd layer. The second deposit of Ta takes place in the presence of oxygen to create a dielectric layer of Ta_2O_5. The layering which is created in the end is TaN, Ti, Pd, Ta_2O_5 and Pd, of which the layer of tantalum nitride TaN belongs to the resistors and the layers of Pd, Ta_2O_5 and Pd belong to the capacitors. The fact
5 that the dielectrics extend beyond the edge of the corresponding upper electrodes allows good insulation between the opposing electrodes.

As may be seen, with respect to the method of A. Chu, the two interface layers between the Ta_2O_5 and the palladium electrodes of the capacitors are no longer necessary because the mechanical stability of the structure of the capacitors is
10 perfectly assured by the thick gold crowns corresponding to the metallizations grown galvanically in contact with the lower electrodes and close to the dielectrics, and by special provisions used in the sputtering phase of the layering of the base film as discussed below.

The structural strengthening is essentially due to the fact that the above
15 mentioned crowns are firmly anchored to the underlying metallizations, thanks to the electrolytic growth and also shut up and lock the dielectrics while forming therewith hermetic joints. The existence of similar crowns is not the result of the above mentioned process nor of any of which we have knowledge. In the process of A. Chu, as appears from the figures, it can be seen that the metallization connecting the lower
20 electrode to the rest of the circuit does indeed grow close to the dielectric but does not form a crown surrounding it and is absent in the zone underlying the air bridge connecting the upper electrode to the remaining circuit.

From tests performed in the applicant's laboratories on capacitors which differed from those created by the subject method only in that the gold crown
25 metallization did not close around the dielectric, structural flaking off was observed with detachment of the Ta_2O_5 from the palladium of the lower electrode starting from the zone in which the crown did not close. This shows need of the crown, which strengthens the structure of the capacitors, and improves the electrical conduction to the lower electrodes, because it reduces their equivalent series resistance, thanks to
30 a more efficient charge injection at the interface with the dielectric and to a more uniform distribution of current density on the surface of the lower electrodes. For the sake of brevity the proof of these assumptions, which were observed experimentally in the applicant's laboratory, is left out.

Further remarks regarding the total equivalent series resistance values
35 created by the method in accordance with the present invention better justify the low values obtainable. Among these remarks are, 1) the palladium of the electrodes already has low resistivity per se, 2) the deposit of interface layers is not provided

between the dielectric and the electrodes, 3) the low resistance of the thin layer of palladium belonging to the upper electrode is further reduced by the presence of a thick overlying gold layer, 4) the thickness of the palladium layer of the lower electrode is double that of the upper electrode, and 5) there is present a thick gold crown
5 anchored to the lower electrode.

The advantages of the subject process are thus amply justified in the provision of integrated capacitors for microwave applications and to these is added the advantage of a greater simplification with respect to the known methods and due overall to the fact that the resistors and capacitors are created by subtraction starting
10 from layers deposited by sputtering in an initial phase without breaking the vacuum cycle. The specific advantage of the use of a single vacuum cycle is to be able to operate in a low-contamination environment and this implies greater integrity of the dielectrics of the finished capacitors and ultimately better production yield.

Further purposes and advantages of the present invention are clarified in the
15 detailed description of an embodiment thereof given below by way of explanatory nonlimiting example and whose principal production phases are explained sequentially in FIGS 2 to 23 of the annexed drawings wherein for ease of representation the dimensions of the elements shown do not correspond to the real dimensions.

20 FIG 1 is a top view of a portion of the thin-film circuit as it appears at the end of the manufacturing process explained in the remaining FIGS In the FIG can be seen a substrate 1 supporting a resistor RES, a capacitor CAP and a connecting air bridge ABR placed between the two and partially superimposed on both.

The resistor RES consists of a resistive path 1r which breaks a conductive
25 path 1c1 of which are also part the two terminals of RES, one of which is connected to one end of ABR and the other is broken on the left side of the FIG.

The capacitor CAP consists of an upper electrode ES superimposed on a dielectric DL which is in turn surrounded by a metallization COR as a crown completely superimposed on an equivalent portion of lower electrode which extends
30 beyond the edge of the dielectric DL and consequently the lower electrode is hidden in the FIG. The crown COR belongs to a conductive path 1c2 which is broken on the right-hand side of the FIG. The upper electrode ES is in a central position with respect to the dielectric DL and has a smaller surface area than it, which is in turn surrounded by the crown COR. Therefore the bridge ABR bridges the dielectric DL
35 and the crown COR and connects with the electrode ES to complete the series connection between CAP and RES. As set forth in the explanation of the following FIGS the conductive paths 1c1 and 1c2, the crown COR and the terminals of RES

belong to a single conductive layout.

FIG 1 also shows an axis A-A which represents the trace of a plane of cut perpendicular to the substrate 1 along the center line of RES, ABR and CAP. The following FIGS from 2 to 23 refer without distinction to either of the two cross sections specular with respect to the axis A-A. The reference to the layout of FIG 1 in the above mentioned FIGS does not limit the process described through them and this allows creating the complete resistive, capacitive and conductive layout.

In FIG 2 can be seen no less than 5 superimposed layers indicated in order by 2, 3, 4, 5 and 6 and consisting predominantly of metallic material deposited on one side of the substrate 1 (termed hereinafter 'front'). Deposit of all the layers is performed by means of cathode vacuum metal 'sputtering', without breaking the vacuum cycle as better explained below. Since for the success of the process it was observed experimentally that the surface of the substrate 1 must be perfectly smooth, the choice of the material fell in a non-limiting manner on Corning glass 7059. It is however possible to use other known insulating materials such as e.g. alumina, sapphire, etc. In this case the substrates must be lapped or leveled if necessary by means of appropriate known processing.

The layer 2 adhering to the substrate 1 consists of resistive metal, e.g. tantalum or its compounds with nitrogen or nitrogen and oxygen. Tantalum nitride TaN is indicated below in a nonlimiting manner. The layer 3 consists of a good conducting metal with adhesive characteristics such as e.g. titanium. The layers 4 and 6 consist of the same good conducting metal having antidiffusive behaviour, e.g. palladium. The layer 5 consists of dielectric material, e.g. tantalum pentoxide Ta_2O_5.

The thickness of the layers 2, 3, 4, 5 and 6 of the nonlimiting example, that is TaN, Ti, Pd, Ta_2O_5 and Pd is respectively 0.1, 0.05, 0.5, 0,4, 0.25 μm. As may be seen, the layer 4 of Pd has a thickness double that of the Pd of layer 6. This provision serves to reduce the resistance value of the layer 4 from which will be made the lower electrode of the capacitor CAP (FIG 1) since this electrode is not in contact with the thick gold crown COR (FIG 1) in the zone underlying the dielectric.

For the sake of drawing convenience, in FIG 2 there is not shown on the back side of the substrate 1 an extended metallization acting as a ground plane. This metallization is performed in a separate vacuum cycle before deposit of the layers visible on the front side. The above mentioned metallization consists of a 0.05 μm layer of titanium deposited by sputtering directly in contact with the substrate 1. There follows a 0.25 μm layer of palladium grown in contact with the previous one in the same vacuum cycle. In an appropriate phase of the process, which is explained below, there is grown galvanically a gold layer in contact with the palladium layer to

complete the ground plane. It is now also possible to integrate the process of the example with one of those known which allow creating ground deposits through metallized holes. For this purpose it is expedient to use the 'Process for the production of metallized holes in dielectric substrates comprising conductive and/or resistive paths in thin film interconnected with each other' described in European patent application no. 94117039.1 filed in the name of the same applicant. The most expedient point at which to activate the above mentioned process is indicated below.

The layering of FIG 2 allows only the subtractive creation of resistors and capacitors. This being the case, layer 2 taken alone constitutes the material of the resistive path which characterizes the resistor RES of FIG 1. Taken together with layers 3 and 4 it contributes to provision of the conductive paths. It is clear that to provide layers 2, 3, 4, 5 and 6 there can be used all those materials having similar electrical and physical characteristics whose use is known in thin-film technology.

Layers 4, 5 and 6 are part of the structure of the capacitor CAP and specifically the layers of Pd 4 and 6 belong respectively to the lower and upper electrodes of CAP and the layer 5 of Ta_2O_5 created as shown below belongs to the dielectric thereof.

At this point it is appropriate to clarify what was said in the introduction about the use in the subject process of particular provisions aiding adhesion between the Ta_2O_5 layer and the Pd layer. For this purpose it is useful to first describe briefly the deposition equipment, for which, for the sake of brevity, no figure is presented. As known, this equipment consists of a chamber in which are located the substrates to be metallized and placed on an appropriate plate and one or more metal disks, termed below 'targets', which will supply the material to create the layering of FIG 2. The interior of the chamber is kept under very hard vacuum by a high-vacuum pump having high pumping speed. It is however possible to introduce small gaseous flows having adjustable flowrate. The chamber is also equipped with all those sensors and actuators indispensable for accurate control of the deposit process. The plate and targets are connected to the terminals of a direct-current generator having rather high bias so that the whole assembly takes on a configuration similar to that of a diode with the cathode connected to the target and the anode connected to the substrate-holding plate. In series with the direct-current generator there can also be located a radiofrequency current generator with adjustable power. In the chamber is introduced an argon flow which is immediately ionized by the electrical field. The argon ions accelerated by the field violently strike the target connected to the cathode, removing the surface atoms, which are deposited on the substrates to metallize them. The movement of the ions in the chamber is equivalent to a current circulating

between the generator electrodes. To aid metallization there can be applied to the substrate-holding plate a rotating movement with adjustable speed. The presence of several targets allows deposit of several superimposed metallic layers without having to open the chamber each time to change the target and break the vacuum. The
5 presence of an electric heater allows changing the temperature of the substrates.

Even while keeping plasma production triggered, it is possible to prevent the metallic atoms of the target from reaching the substrates by inserting between the target and the substrate-holding plate a lamination termed hereinafter 'shutter'. This condition, termed hereinafter 'presputtering', has the purpose of taking the sputtering
10 process to rated operation.

By using the same equipment it is also possible to perform surface treatments on substrates already metallized, an operation termed hereinafter 'etching'. A procedure designed for this purpose consists of closing the shutter to create the plasma merely by turning on the radiofrequency generator. Under these conditions
15 the argon ions accelerated by the electrical field with radiofrequency strike the substrates and modify the surface morphology of the metallization.

The metal deposit or surface treatment operations described above involve mechanisms of an essentially physical nature. It is however possible to conjugate these mechanisms with those typical of chemical reactions to secure different
20 advantages, among which the most important is that of being able to deposit compounds in addition to the metallic atoms, for example, the resistive compound of TaN or the dielectric compound of Ta_2O_5. The above mentioned procedure, termed hereinafter 'reactive sputtering', is clarified below for the process steps in which it is applied.

25 Now returning to the remarks made above on the existence of particular provisions introduced in the basic film sputtering phase, it is noted that their purpose is to aid adhesion between the Ta_2O_5 and the two Pd layers between which it is inserted. Therefore they are applied starting from the completed deposit of the lower layer 4 of Pd and comprise in succession the phases of:

30 - heating of the substrate 1 to approximately 100° C for 7';

- presputtering for approximately 8' of the Ta target secured by closing the shutter to prevent metallization of the substrate 1 and introducing into the chamber a mixture of argon and oxygen and starting plasma production; the purpose is to appropriately condition the Ta target by taking it as near as possible to the condition it
35 will achieve during the deposit phase so that the characteristics of the film deposited thereafter will be uniform from the start;

- surface treatment of the layer 4 of Pd and consisting of a limited etching in

plasma of argon ions lasting only 2' and supported by a radiofrequency power of approximately 30 mW/cm^2 with the purpose being to "roughen" the Pd surface and thus aid anchoring of the Ta_2O_5 layer which will subsequently be grown; and

- additional presputtering of the Ta target similar to the previous one but

5 lasting approximately 4'.

There then follows the actual sputtering of the Ta_2O_5 of the layer 5 performed by merely opening the shutter because working conditions remain identical to those of the preceding presputtering phase. Accordingly the sputtering of the Ta_2O_5 is the reactive type and is performed by introducing oxygen in the chamber

10 during the tantalum sputtering.

By adopting appropriate values of the variables characterizing this sputtering phase, the whole of which is termed 'point of work', it was possible to secure the deposit of an amorphous film whose composition is near stoichiometric (O/Ta =2.5). Such a film possesses excellent dielectric characteristics while the capacitor resulting

15 therefrom possesses low loss currents and high break-down voltages. The work point is defined in a non-limiting manner by the following values:

- S_{N2} = 485 l/s (pumping speed of the high-vacuum pump for nitrogen under standard conditions of 25 °C e 1.01 x 10^5 Pa),
- Q_{Ar} = 60 sccm (flow of Ar expressed in cubic centimeters per minute under

20 standard conditions);

- Q_{O2} = 46 sccm (flow of oxygen under standard conditions);
- p_{tot} = 0.41 Pa (total pressure in chamber);
- I = 3.7 A (electric current supported by the plasma);
- h = 100 mm (distance between targets and substrates); and

25 - V_ω = 1.05 rad/s (angular velocity of the substrate-holding plate).

With the provisions preceding the sputtering of the Ta_2O_5 of layer 5 the adhesion between the layer 4 of Pd and the layer 5 of Ta_2O_5 proved good.

Concerning the adhesion between the Ta_2O_5 layer 5 and the Pd layer 6 the only provision adopted was to precede the deposit of the layer 6 of Pd by a plasma

30 treatment of the surface of the layer 5 of Ta_2O_5 consisting of a limited argon etching lasting only 2' while using a radiofrequency power of approximately 30 mW/cm^2 as done previously for the Pd layer 4.

After creating the layering of FIG 2 the substrates are washed with a chromic mixture, rinsed and then dehydrated at 150° C for 15'.

35 With reference to FIG 3 the conductive layer 6 is first covered uniformly with an emulsion 7 photosensitive to ultraviolet rays (termed hereinafter 'photoresist') over which is applied a mask (not shown in the figures) which is opaque to the radiation in

a zone outside the surface of the upper electrode ES (FIG 1) of the capacitor CAP. This corresponds to the use of a positive photoresist 7, i.e. which depolymerizes in the part exposed to radiation. The photoresist 7 is exposed to the ultraviolet light through the mask and then developed chemically to eliminate the depolymerized part during
5 development. If metallization of the ground plane is present on the back side of the substrate 1, it also must be protected by photoresist 7 to avoid the growth of gold during the next phase.

With reference to FIG 4, in the zone of the palladium layer 6 free of photoresist 7 there is grown galvanically a thickness of gold 8 of 2 to 3 μm.

10 With reference to FIG 5 the residual photoresist is removed chemically everywhere and the substrates are then washed in a chromic mixture and carefully rinsed.

With reference to FIG 6 the Pd layer 6 is removed outside the gold 8 by means of chemical etching in a solution based on $FeCl_3$ and 40% HF which does not
15 corrode the Ta_2O_5 5 of the gold 8. The etching time of the Pd 6 is short (approximately 2') to limit the effect of under-etching on the edge of the gold 8 and resulting reduction of the capacitance of the capacitor. The substrates are then washed in a chromic mixture, carefully rinsed and dehydrated at 150° C for 15' to create the upper electrode ES of the capacitor.

20 With reference to FIG 7 the layer 5 of Ta_2O_5 is covered with photoresist 9, exposed with mask and developed to create the covering of the surface delimiting the dielectric DL (FIG 1).

With reference to FIG 8 the layer 5 of Ta_2O_5 is removed outside the zone of the dielectric DL by using for the purpose equipment similar to that described for the
25 sputtering of the layers 2, 3, 4, 5 and 6, but in this case the targets are missing and in addition the substrate-holding plates are directly connected to a terminal of an appropriate radiofrequency current generator. Recalling what was said about the reactive sputtering, even in case of plasma etching it is possible to give the process a chemical in addition to physical nature by using to produce the plasma an appropriate
30 gas forming volatile compounds with the material to be removed (reactive ion etching - RIE). The etching of the layer 5 of Ta_2O_5 is performed in plasma of freon 14 (CF_4), with the use of this gas not being limiting in itself. During the bombardment more kinetic energy is conferred on the ions than that of the preceding surface treatments performed during the metallization operations of the substrate 1. The presence of a
35 privileged direction of the incident ions confers on the plasma etching an anisotropic nature as opposed to the isotropy of a possible chemical etching in a liquid solution which allows limiting underengraving effects.

With reference to FIG 9 the residual photoresist 9 is removed to create the dielectric DL. There follows a phase of washing, rinsing and dehydration similar to the preceding ones.

With reference to FIGS 10 and 1 the layer 4 of Pd is covered with photoresist 10, exposed with a mask and developed to create zones free of photoresist 10 opposite the conductive paths 1c1 and 1c2, the resistive path 1r, and the lower electrode outside the dielectric DL.

With reference to FIGS 11 and 1 there is grown galvanically a thickness of gold 11 of approximately 5 μm on the zones of the layer 4 of Pd free of the photoresist 10. The gold grows uniformly on the Pd 4 to form the conductive paths 1c1 and 1c2 and the crown COR and covering the resistive path 1r. On the upper electrode there is no further growth of gold in this phase, since the palladium 4 isolates the overlying gold 8 from the electrodes of the galvanic bath. In this phase the gold 11 grows galvanically even on the back side of the substrate 1 in contact with the existing palladium layer to improve the electric conductivity of the ground plane previously consisting of only the of titanium and palladium layers.

With reference to FIG 12, the residual photoresist 10 is removed everywhere and if necessary from the back also, and the substrate is carefully washed and rinsed.

The following FIGS 13, 14 and 15 concern removal of the layers 2, 3 and 4 of TaN, Ti and Pd respectively outside the electrolytic gold 11 to bare the surface of the substrate 1 to completely separate the conductive path 1c1 from the capacitor CAP. The removal can be performed chemically by using acid solutions which do not corrode the gold and the Ta_2O_5, or dry with the aid of plasmas having also selective chemical action (RIE). As regards the chemical etching, it would theoretically be possible to avoid protection of the capacitor CAP because the crown COR encloses the dielectric DL to form therewith a hermetically sealed joint for the acid solution, which thus cannot penetrate and corrode the metallizations 2, 3 and 4 of the lower electrode EI.

With reference to FIG 13 it was considered expedient to protect with a thickness of photoresist 12 the upper electrode ES and the dielectric DL of the capacitor, to prevent the acid solution from engraving the Pd 6 along the edge underlying the gold 8 to alter the capacitive value of the capacitor. The protection supplied by the photoresist 12 proves suitable even when there is used a plasma reactive etching instead of the chemical one. In this case it would avoid possible partial removal of the Ta_2O_5 belonging to the uncovered crown of the dielectric DL extending beyond the edge of the upper electrode ES. On the other hand it is observed that the protection provided by the photoresist 12 would not be necessary if

there were available acid solutions without underetching effect or if there were no need for high precision in the capacitance value of the capacitor.

FIG 14 shows how the substrate 1 appears at the end of the chemical etching of the metallizations of the layers 2, 3 and 4 in the unprotected zones and FIG 15 shows the same substrate as in FIG 14 after removal of the residual photoresist 12.

As may be seen in FIG 15, the metallization of the crown COR keeps the capacitor CAP completely included in the conductive path 1c2 to form therewith a very compact structure which, while subjected to very severe environmental conditions characterized e.g. by the presence of mechanical vibrations or broad temperature ranges, never showed any mechanical failure or degradation in electrical operation.

The following FIGS 16, 17 and 18 refer to the creation of the resistor RES.

With reference to FIG 16 the substrate is covered with a layer of photoresist 13, exposed with a mask and developed to create a zone free of photoresist opposite the resistive path 1r of FIG 18. If on the back of the substrate 1 there is present the gold ground plane it also must be protected with photoresist 13 to avoid removal thereof during the next phase.

With reference to FIG 17 the layers of gold 11, palladium 4 and titanium 3 remaining uncovered by the photoresist 13 are removed with selective acid solutions which leave unchanged only the resistive layer 2 of TaN. After removal of all the residual layer of photoresist 13 there is created the circuit of FIG 18 in which is seen the resistor RES separated from the capacitor CAP. The circuit is however still not finished because there remains to be completed the connection of the upper electrode of CAP with the adjacent terminal of RES by means of the air bridge ABR of FIG 1.

Before growth of the metallic bridge ABR and if the circuit requires it it is possible to provide holes in the dielectric substrate 1 which allow the connections to the ground plane using the process for metallization thereof as mentioned above.

In the remaining FIGS 19, 20, 21, 22 and 23 there is illustrated the provision of the metallic bridge ABR (FIG 23).

With reference to FIG 19 the substrate 1 is covered with a layer of photosensitive polyimide 14 having the purpose of providing the frame of the bridge ABR (FIG 23). The polyimide 14 is exposed with a mask and developed to act as a photoresist by making openings where it is wished to make the piers of the bridge and in contact with the gold 11 of the resistor terminal and the gold 8 belonging to the upper electrode of the capacitor respectively.

With reference to FIG 20, on the entire surface of the residual polyimide

there is deposited a thin conductive metallization for service 15 consisting of TiN and Au in such a manner as to allow electrolytic growth of gold in the subsequent phases.

With reference to FIG 21, on the entire surface of the metallization 15 there is deposited a layer of photoresist 16 which is exposed with a mask and developed to create a zone free of photoresist 16 which will be occupied by the bridge ABR (FIG 23). If on the back of the substrate 1 there is the metallization of the ground plane this also must be protected with photoresist 16 to avoid further growth of gold during the following phase.

With reference to FIG 22 a thickness of gold 17 is grown electrolytically in contact with the metallization 15 which is not covered by the residual photoresist 16. The gold 17 grows until completion of the bridge ABR.

With reference to FIG 23 the polyimide 14 and the photoresist 16 are removed everywhere to create the complete circuit consisting of the series connection of the resistor RES with the capacitor CAP which is implemented through the air bridge ABR.

With reference to the above FIGS there is now explained a small variant which avoids the initial growth of the gold 8 (FIG 4) opposite the upper electrode of the capacitor while combining this growth with that of the air bridge ABR (FIG 23). For this purpose and with reference to the process phase illustrated in FIG 3 it is necessary to protect with the photoresist 7 the Pd surface of the layer 6 corresponding to that of the upper electrode ES (FIG 1). This is a zone which is complementary to the protected one illustrated in FIG 3. After this, avoiding the phases illustrated in FIGS 4 and 5, all the remaining phases of the process illustrate in FIGS 6 to 18 remain unchanged. It is clear that the gold layer 8 will not appear in the above mentioned FIGS The phases which concern the fabrication of the bridge ABR and illustrated in FIGS 19 to 23 must be modified in such a manner as to cause the dimensions of the pier on the capacitor to coincide with those of the upper electrode ES unless there are tolerances in the centering of the masks.

CLAIMS

1. Manufacturing process for thin film circuits on a dielectric substrate and characterized in that it comprises in succession the steps of:

a) vacuum cathode sputtering of metals which are deposited on said substrate (1) to form a succession of superimposed layers of which a first layer (2) has resistive electrical characteristics, a second layer (3) is a good conductor with adhesive properties, a third layer (4) is a good conductor with antidiffusive properties, a fourth layer (5) has dielectric characteristics, and a fifth layer (6) has the same characteristics as the third;

b) covering of the metallized substrate (1) with a layer of a photosensitive lacquer (7) termed hereinafter 'photoresist', masking of zones corresponding to the positions of upper electrodes (ES) of capacitors (CAP), exposure and development to create zones of said fifth metallic layer (6) free of photoresist opposite the masks;

c) galvanic growth of metal (8), removal of the residual photoresist (7) and removal of said fifth metallic layer (6) outside said metal (8) grown galvanically to create said upper electrodes (ES);

d) covering with photoresist (9) of said substrate (1), masking of zones which include said upper electrodes (ES), exposure and development to create zones of said dielectric layer (5) free of photoresist outside the masks;

e) removal of said dielectric zones free of photoresist and removal of the residual photoresist (9) to create dielectrics (DL) of said capacitors (CAP) extending beyond the edge of said upper electrodes (ES);

f) covering with photoresist (10) of said substrate (1), masking of zones corresponding to lower electrodes (EI) of said capacitors (CAP) with said zones including the surfaces of said dielectrics (DL) and masking of zones corresponding to conductive paths (1c1,1c2) and resistive paths (1r), exposure and development to create zones of said third metallic layer (4) free of photoresist (10) opposite the masks;

g) growth of metal (11) galvanically opposite said conductive paths (1c1,1c2) and said resistive paths (1r) and on the surface of said lower electrodes (EI) extending beyond the edge of said dielectrics (DL) with said metal (11) growing near to said edges to form a crown (COR) hermetically enclosing the dielectrics (DL) and mechanically stabilizing the structure of the capacitors (CAP) and facilitating the conduction of current to the lower electrodes (EI); and

h) removal of the residual photoresist (10) and removal of residual metallic layers (2,3,4) outside said metal (11) grown galvanically to create conductive lines (1c1) superimposed on said resistive paths (1r) to form a single unit with said metallic

crown (COR) grown over said lower electrodes (EI);

i) covering with photoresist (13) of said substrate (1), masking of zones corresponding to said resistive paths (1r), exposure and development to create zones of said conductive lines free of photoresist opposite said resistive paths (1r);

5 l) removal of material (11,4,3) opposite said zones free of photoresist excepting the metal belonging to said first resistive layer (2) and removal of the residual photoresist (13) to create resistors (RES); and

m) growth of metal (17) galvanically opposite metallic air bridges (ABR) connecting said upper electrodes (ES) to said conductive paths (1c1) or to terminals

10 of said resistors (RES).

2. Manufacturing process in accordance with claim 1 and characterized in that:

- said first layer (2) with resistive electrical characteristics is tantalum or tantalum doped with nitrogen or with nitrogen and oxygen;

- said second layer (3) which is a good conductor with adhesive properties is

15 titanium;

- said third layer (4) which is a good conductor with antidiffusive properties is palladium;

- said fourth layer (5) with dielectric characteristics is tantalum pentoxide (Ta_2O_5); and

20 - said fifth layer (6) is palladium.

3. Manufacturing process in accordance with claim 1 and characterized in that said metal (8,11,17) grown galvanically in said phases c), g) and m) is gold.

4. Manufacturing process in accordance with claim 1 and characterized in that said third layer (4) has a thickness double that of said fifth layer (6).

25 5. Manufacturing process in accordance with claim 1 or 2 and characterized in that said phase a) of vacuum cathode sputtering of metals on said substrate (1) is completed without breaking the vacuum cycle and in that the deposit of said fourth dielectric layer (5) is preceded by appropriate subphases introduced to aid adhesion between said third (4) and fourth (5) layers whose sequence is as follows:

30 a1) heating of said substrate (1) to approximately 100° C for 7';

a2) surface treatment of one such metal which is sputtered later to deposit said fourth dielectric layer (5) and taking the surface back to a condition as near as possible that reached by the same metal during deposit of said fourth layer (5);

a3) surface treatment of said third layer (4) to roughen its surface and aid

35 anchoring of said fourth dielectric layer (5) subsequently deposited; and

a4) surface treatment of said metal which is subsequently sputtered similarly to that of said subphase a2) but lasting half as long.

6. Manufacturing process in accordance with claim 1 or 2 and characterized in that said vacuum cathode sputtering of metals is, a) completed without breaking the vacuum cycle and in that the deposit of said fifth layer (6) is preceded by a subphase a5) in which is completed a surface treatment of said fourth dielectric layer (5) designed to aid adhesion between said fourth (5) and fifth (6) layers.

7. Manufacturing process in accordance with claim 1, 2 or 5 characterized in that said vacuum cathode sputtering of metals a) is completed without breaking the vacuum cycle and in that the deposit of said fourth dielectric layer (5) takes place by introducing oxygen in the vacuum chamber during the cathode sputtering of tantalum with the following values of the principal physical variables which control the process during deposit of said dielectric layer (5):

- S_{N2} = 485 l/s where S_{N2} is the pumping speed of a high-vacuum pump used to produce the vacuum in said chamber and where l/s refers to nitrogen under standard conditions of 25° C and $1,01.10^5$ Pa;
- Q_{Ar} = 60 sccm, where Q_{Ar} is a flow of Ar and sccm is a measure of said flow in cubic centimeters per minute under standard conditions;
- Q_{O2} = 46 sccm, where Q_{O2} is a flow of oxygen;
- p_{tot} = 0,41 Pa, where p_{tot} is the total pressure in said chamber;
- I = 3.7 A where I is an electrical current supported by the plasma present in said chamber;
- h = 100 mm where h is a distance between said cathode sputtered tantalum and said substrate (1); and
- V_ω = 1.05 rad/s, where V_ω is the angular velocity of a plate bearing said substrate (1).

8. Manufacturing process in accordance with claim 5 and characterized in that said surface treatment implemented in said subphase a2) is a cathode sputtering of said metal in the presence of argon and oxygen lasting approximately 8' and in which the deposit of metal on said substrate (1) is prevented.

9. Manufacturing process in accordance with claim 5 and characterized in that said surface treatment implemented in said subphase a3) is a bombardment in plasma of argon ions lasting approximately 2' and supported by a radiofrequency power of approximately 30 mW/cm^2.

10. Manufacturing process in accordance with claim 6 and characterized in that said surface treatment implemented in said subphase a5) is a bombardment in plasma of argon ions lasting approximately 2' and supported by a radiofrequency power of approximately 30 mW/cm^2.

11. Manufacturing process in accordance with claim 1 and characterized in that

said removal phases e), h) and l) include a selective chemical etching.

12. Manufacturing process in accordance with claim 1 and characterized in that at the end of said phase g), said phase h) is preceded by a phase g') in which said substrate (1) is covered with photoresist (12), zones superimposed on said upper electrodes (ES), on said dielectrics (DL) and partially on said metallic crowns (COR) are masked, said photoresist (12) is exposed through the masks and developed to create zones free of photoresist outside the masks with the residual photoresist after development protecting said upper electrode (ES) during said removal of residual metallic layers (2,3,4) performed during said phase h) and being removed at the end thereof.

13. Manufacturing process in accordance with claim 1 or 12 and characterized in that:

- in said phase b) the zones of said fifth metallic layer (6) free of photoresist (7) are created outside the masks;
- in said phase c) said fifth metallic layer (6) is removed outside said masks and there is then removed the residual photoresist (7) to create said upper electrodes (ES); and
- in said phase m) said metal (17) grown galvanically opposite said metallic air bridges (ABR) covers the entire surface of said upper electrodes (ES).

14. Manufacturing process in accordance with any one of the above claims and characterized in that said phase a) is preceded by the deposit of an extensive metallization acting as a ground plane on the face of said substrate (1) opposite that including said thin-film circuits.

15. Manufacturing process in accordance with claim 14 and characterized in that said phase m) is preceded by the provision of metallized holes for the connections to said ground plane.

16. Manufacturing process in accordance with any one of the above claims and characterized in that said substrate 1 is made of glass or a ceramic material appropriately leveled or of any dielectric material having a plane surface.

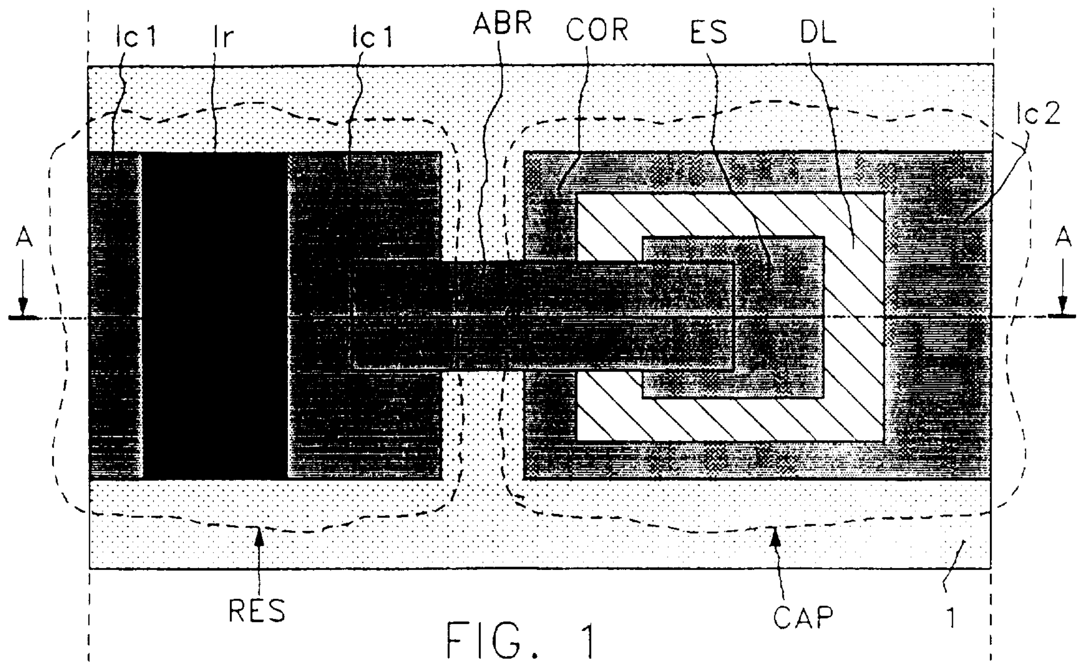

FIG. 1

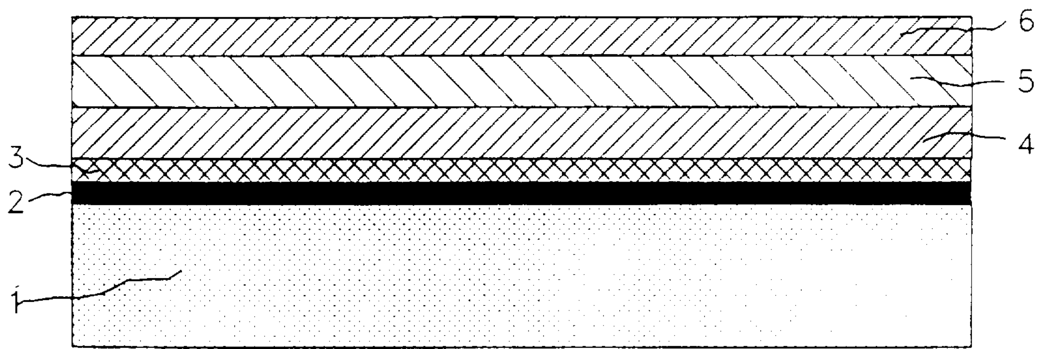

FIG. 2

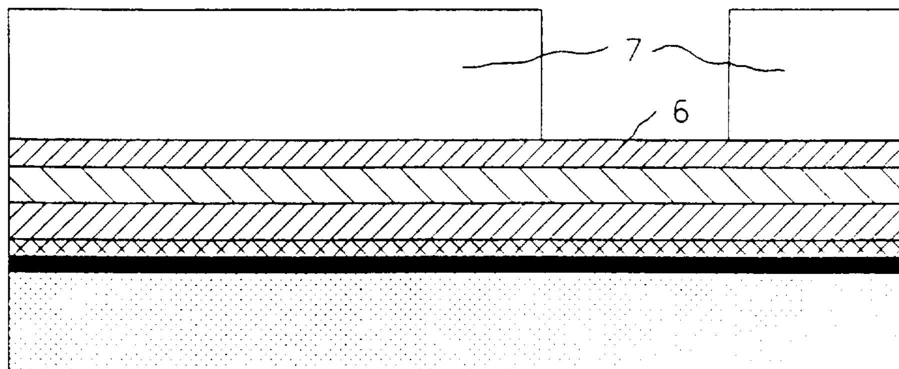

FIG. 3

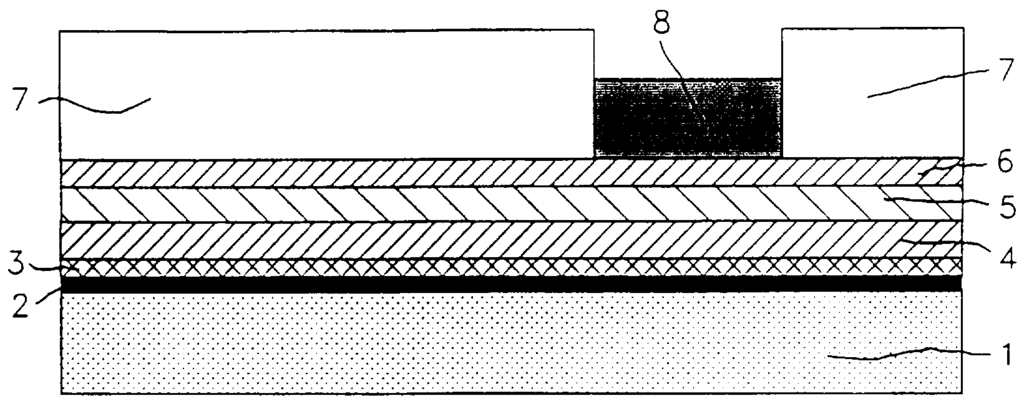

FIG. 4

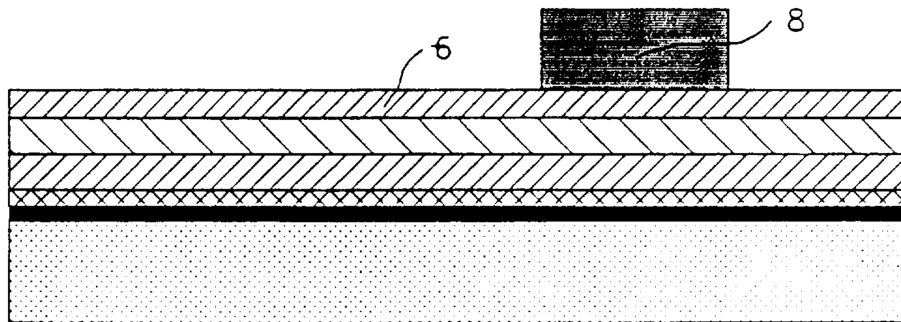

FIG. 5

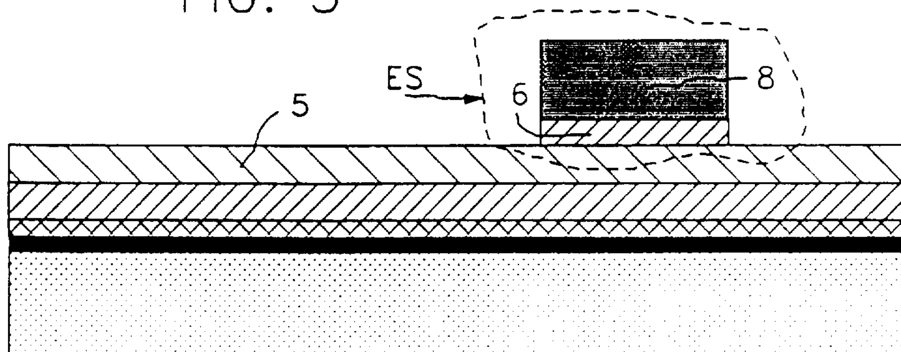

FIG. 6

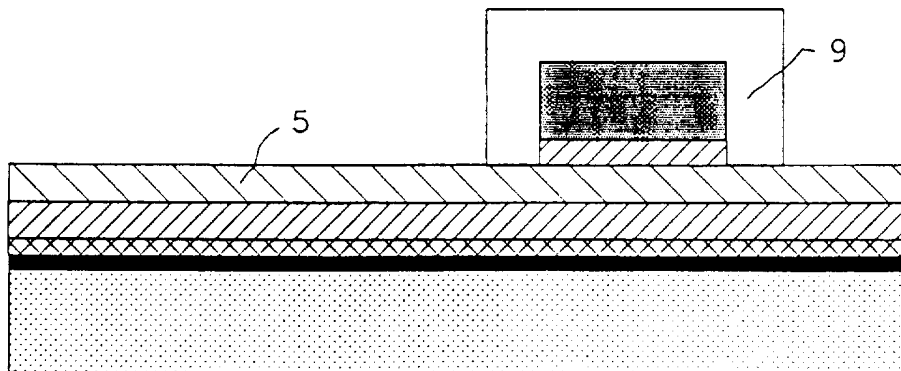

FIG. 7

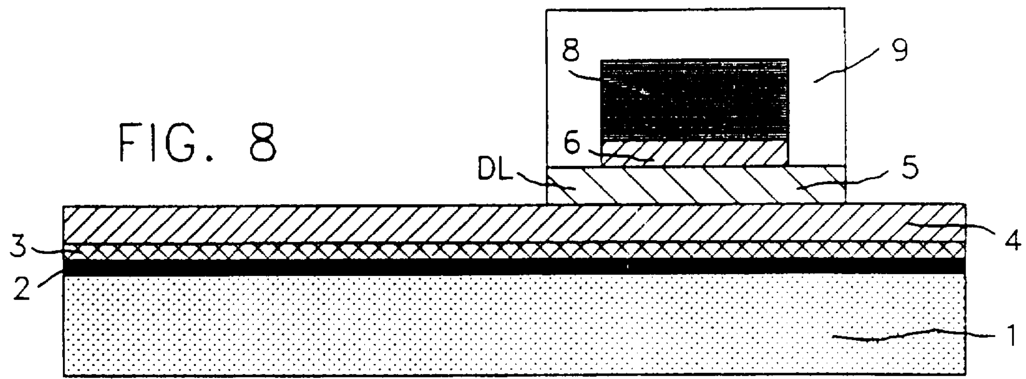

FIG. 8

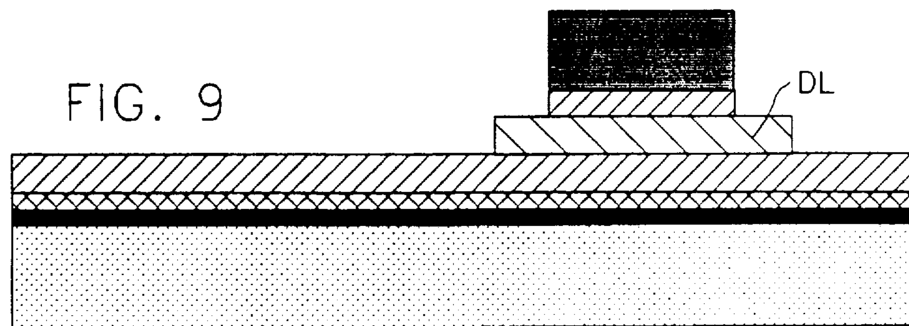

FIG. 9

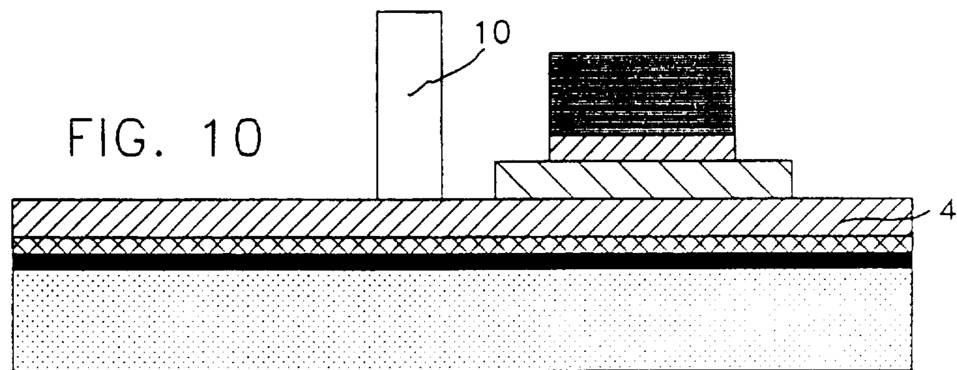

FIG. 10

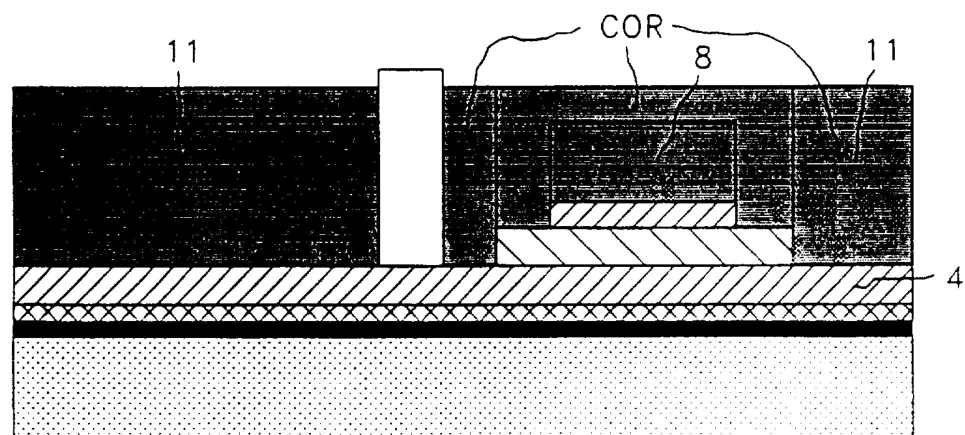

FIG. 11

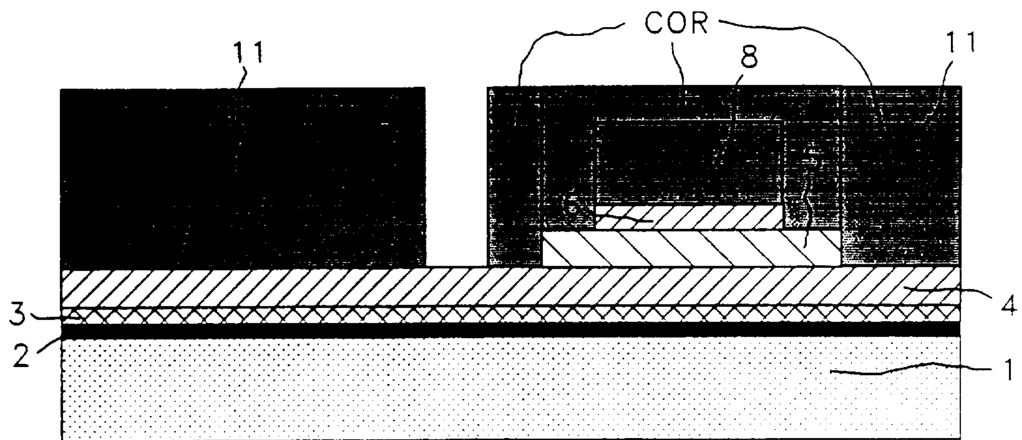

FIG. 12

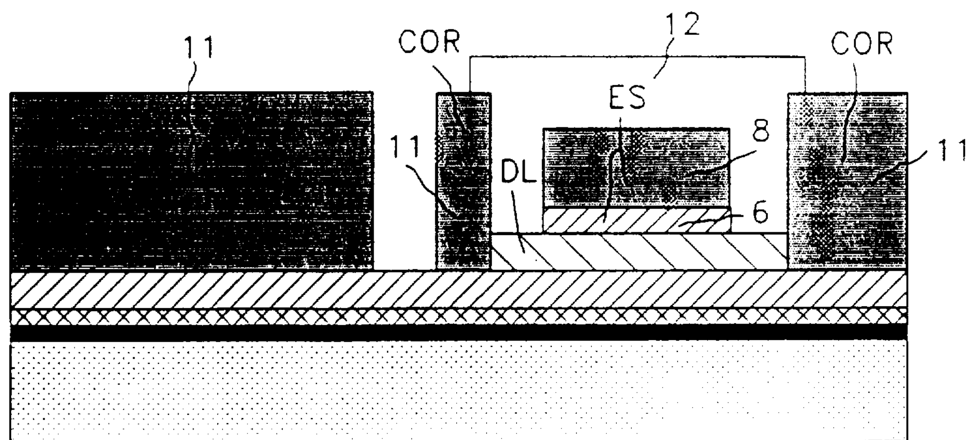

FIG. 13

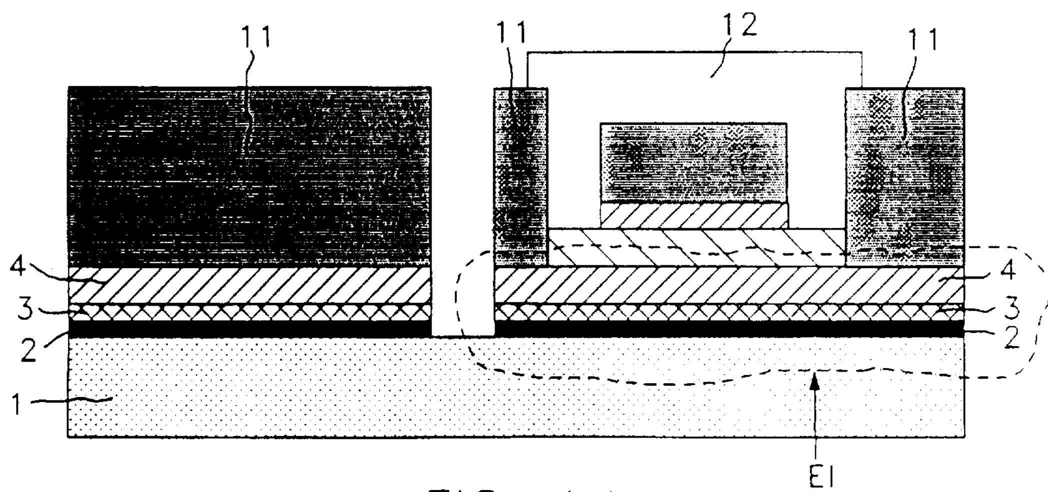

FIG. 14

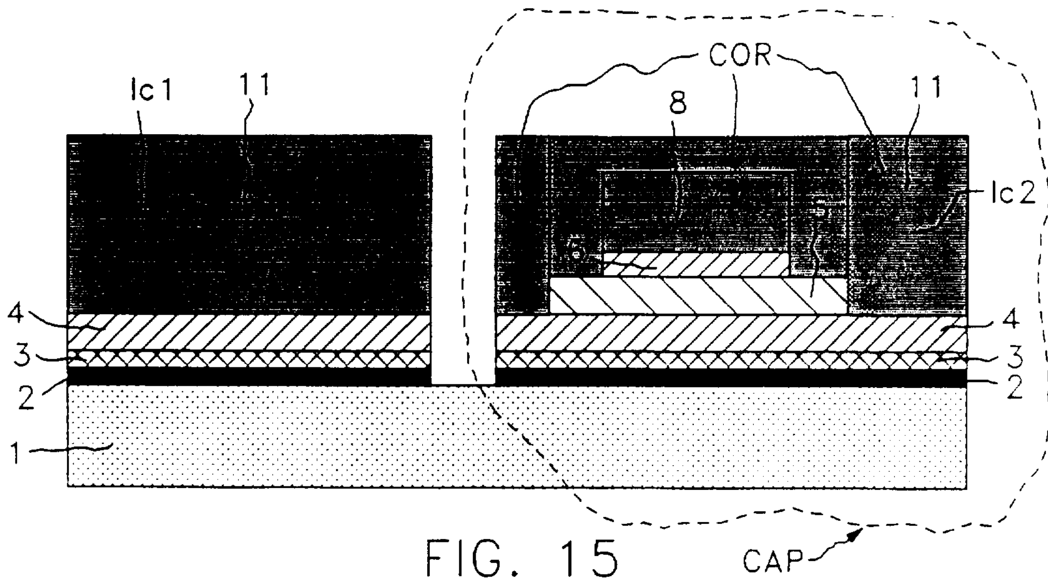

FIG. 15

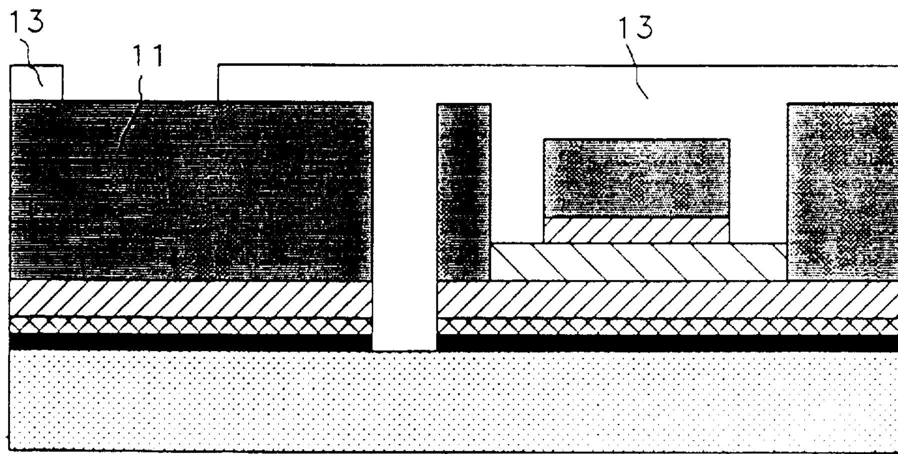

FIG. 16

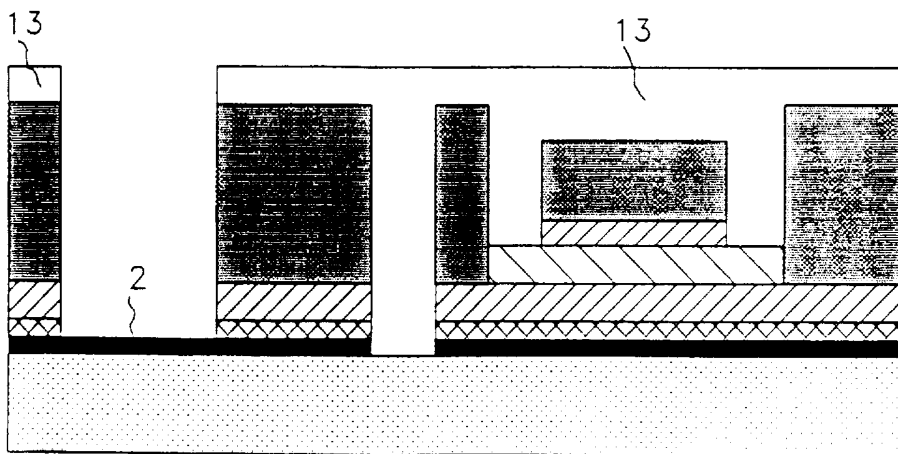

FIG. 17

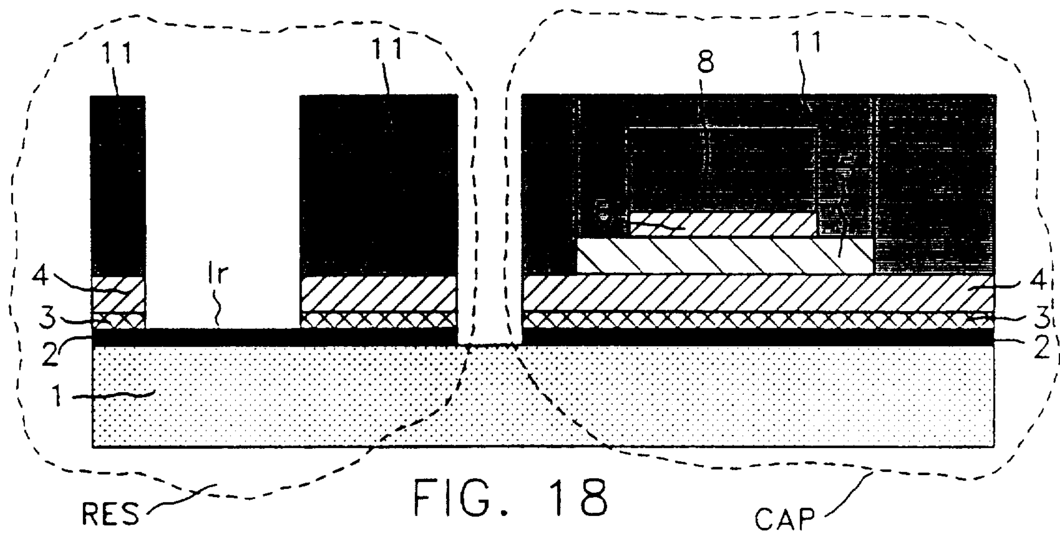

FIG. 18

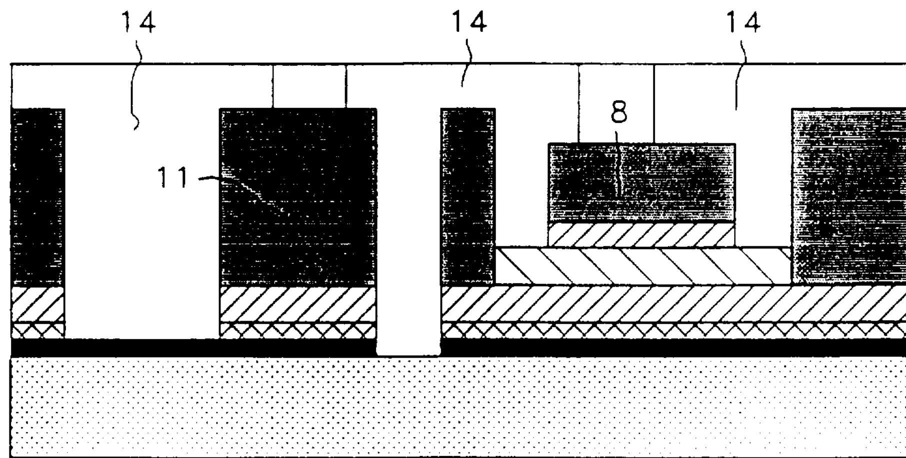

FIG. 19

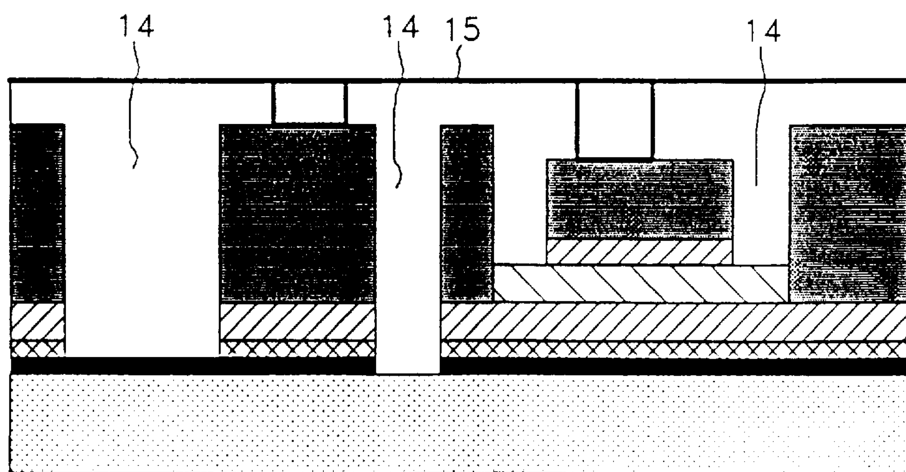

FIG. 20

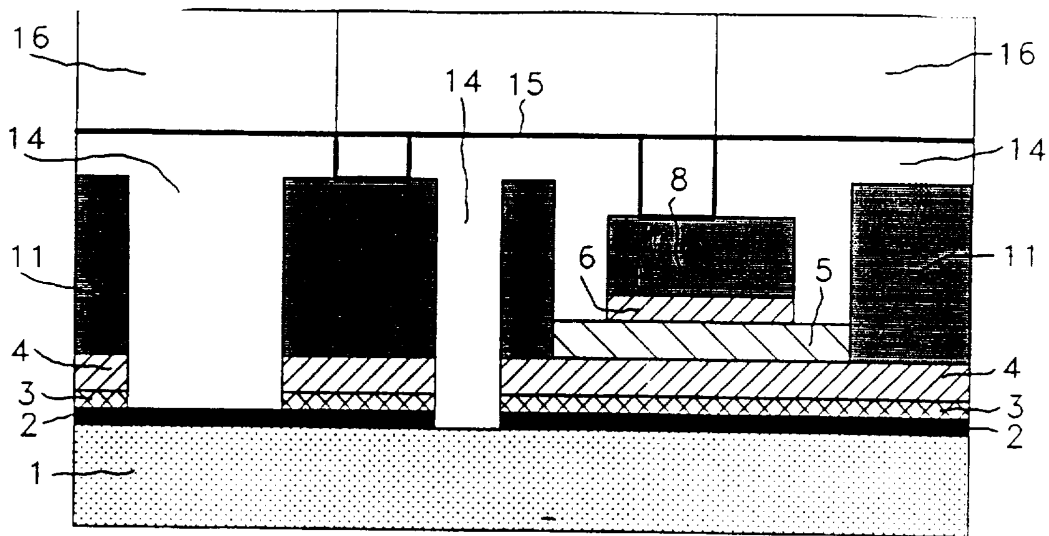

FIG. 21

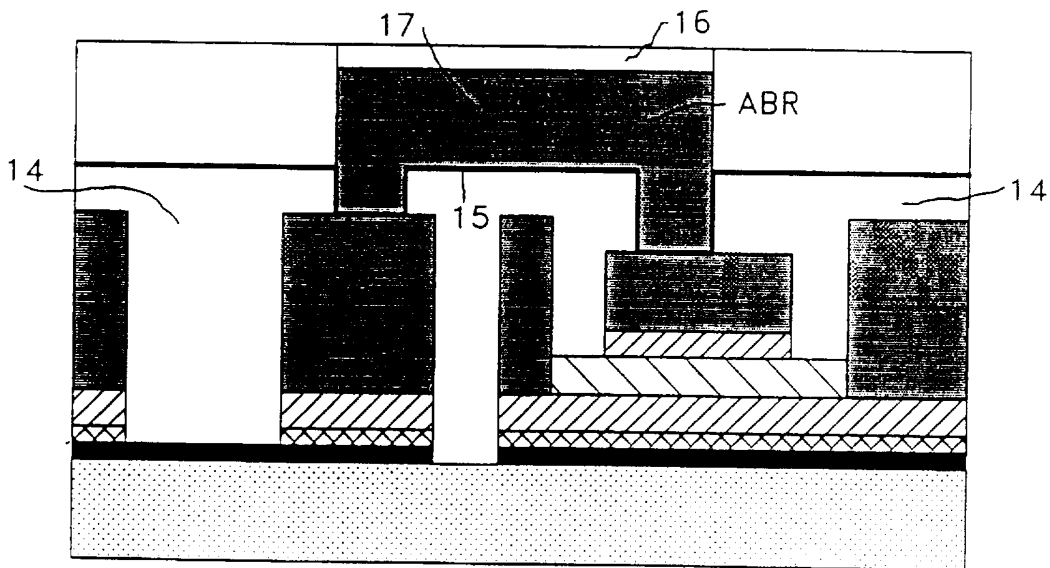

FIG. 22

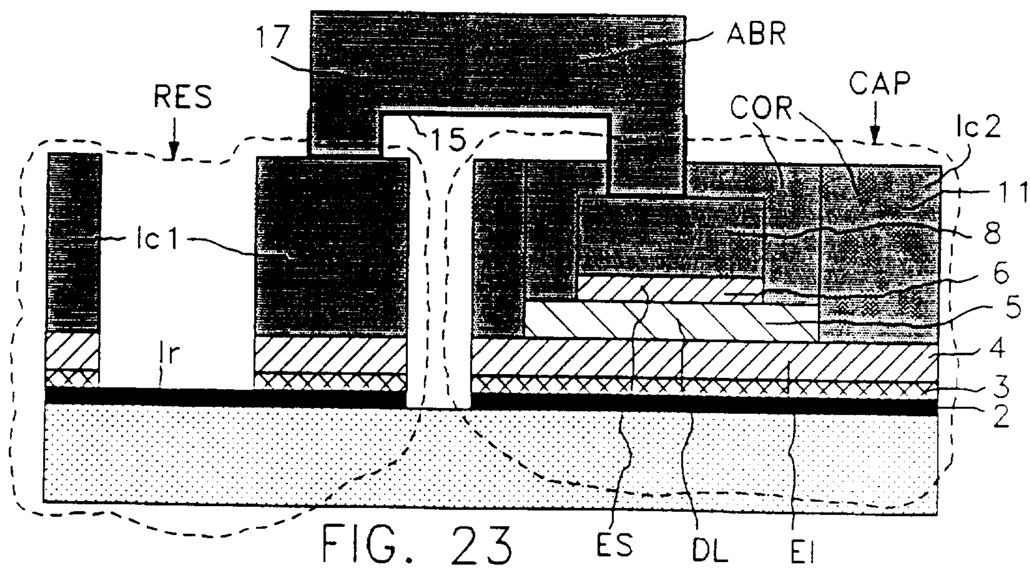

FIG. 23

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/EP 96/04406

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/70 H01L27/01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. ED-30, no. 1, January 1983, NEW YORK US, pages 21-26, XP000611740 A. CHU ET AL.: "A two-stage monolithic IF amplifier utilizing a Ta205 capacitor" cited in the application see page 22, left-hand column, last line - right-hand column, paragraph 1; figure 4 ---	1-3,5,7
A	EP,A,0 670 668 (SIEMENS TELECOMUNICAZIONI SPA) 6 September 1995 cited in the application see the whole document ---	1-3,11, 14-16
A	US,A,4 436 766 (WILLIAMS) 13 March 1984 see the whole document -----	1,3,16

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

2

Date of the actual completion of the international search	Date of mailing of the international search report
22 January 1997	05. 02. 97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Mes, L

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 96/04406

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-670668	06-09-95	NONE	
US-A-4436766	13-03-84	NONE	